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APPLICATION

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TITLE: LOWER PROFILE FLEXIBLE SUBSTRATE PACKAGE FOR ELECTRONIC COMPONENTS

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LOWER PROFILE FLEXIBLE SUBSTRATE PACKAGE FOR ELECTRONIC COMPONENTS

Background

This invention relates generally to flexible substrate packages for electronic components.

Flexible substrate packages, such as polyamide packages, have a flexible substrate sometimes called a flex substrate. Thus, the base cavity is flexible and this can be used for a number of applications, including folded packages.

Polyamide packages generally have an interconnect structure formed within the polyamide substrate. A silicon die is positioned over the polyamide substrate, interconnections are made, for example by wire bonding, and the structure over the polyamide substrate is mold encapsulated. While these structures are advantageously flexible, their vertical profile may be too high for some applications.

Thus, there is a need for lower profile flexible substrate packaging.

Brief Description of the Drawings

Figure 1 is an enlarged, cross-sectional view of one embodiment of the present invention.

Detailed Description

Referring to Figure 1, a flexible substrate packaged semiconductor integrated circuit 10 includes at least one silicon die 24 covered by an encapsulant 36. A flexible substrate core 16, made of polyamide in one embodiment, is coupled to lands 28 on its lower surface in one embodiment. The lands 28 may also be located outside the die shadow area in another embodiment. A series of openings in a covering layer 18 provide for the attachment of solder balls 20 to the lands 28.

The lands 28 may be electrically coupled through an interconnection layer 17 (over the core 16), which in turn electrically couples through vias (not shown) to interconnection layers 19 and 21, contained in buildup layers 12 and 14. Thus, the interconnection structure, made up of the interconnection layers 17, 19, and 21 and the associated vias, may be formed within buildup layers 12 and 14, as opposed to forming them within the substrate core 16. The buildup layers 14 and 12 may be stepped in one embodiment of the present invention so that a cavity 34 is defined which opens up progressively in the stepped fashion.

The integrated circuit die 24 may be attached by a die attach 26 to the polyamide substrate core 16. Thus, the die 24 sits within the cavity 34 within the package 10, defined by the buildup layers 14 and 12. This

configuration may be thermally efficient in some embodiments. In addition, because the interconnection layers 17, 19, and 21 are at least partially removed from the core 16, a lower profile package may be achieved.

While an embodiment is shown with two buildup layers 12 and 14, more buildup layers may be utilized in other embodiments.

In some embodiments, the buildup layers 12 and 14 may be adapted to the thickness of the die 14 so that the upper surface of the die 24 and the upper buildup layer 12 are substantially coplanar. However, in the embodiment illustrated, with a down set configuration between the upper surface of the buildup layer 12 and the upper surface of the silicon die 24, room is provided for wire bonds from contacts 30 on the buildup layer 14 to contacts 32 on the die 24. In another embodiment, flip chip bonding may be provided between the die 24 and the interconnect layers. Also, two dice may be included, with the dice coupled by flip or wire bond interconnections, as two examples.

Thus, in a structure with three interconnection layers 17, 19, and 21, the silicon die 24 may be down set into a cavity 34 providing a thermally efficient lower profile arrangement. The electrical interconnections may be provided through three separate interconnection layers 17, 19, and 21 formed in buildup layers 12 and 14. In some

embodiments, a folded package may be utilized to take advantage of the flexible substrate core 16.

The package 10 may be formed using standard flexible substrate manufacturing steps. When manufacturing a three-plus metal layer flex substrate, a route or punch cavity is formed in the buildup layers 12 and 14. This routing of the cavity can be done in panel or reel-to-reel format, as two examples. The buildup layers are then laminated with the cavity. The top layer may be patterned and then a solder mask may be applied. Thereafter, the typical back end steps, including rinse and bake, may be accomplished.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is: